Processing and Prolonged 500 °C Testing of 4H-SiC JFET Integrated Circuits with Two Levels of Metal Interconnect

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Abstract. Complex integrated circuit (IC) chips rely on more than one level of interconnect metallization for routing of electrical power and signals. This work reports the processing and testing of 4H-SiC junction field effect transistor (JFET) prototype IC's with two levels of metal interconnect capable of prolonged operation at 500 °C. Packaged functional circuits including 3- and 11-stage ring oscillators, a 4-bit digital to analog converter, and a 4-bit address decoder and random access memory cell have been demonstrated at 500 °C. A 3-stage oscillator functioned for over 3000 hours at 500 °C in air ambient. Improved reproducibility remains to be accomplished.

Introduction

Solid state integrated circuits that are capable of *prolonged and stable 500 °C operation* would enable new applications of sensors in the area of aerospace, aeronautics, energy production, and Venus missions [1,2]. An example of this would be placing a high temperature IC inside the package of a sensor directly in the hot section of a gas turbine without the need for water cooling. This would allow enhanced sensing, control, and efficiency. Ideally circuits with medium-scale integration (MSI) levels of complexity (e.g. operation amplifiers, A/Ds, etc.) would be desired for this application. Previously, NASA Glenn has uniquely demonstrated 10,000 hours of 500 °C operation of discrete JFETs and up to 7000 hours of 500 °C operation for simple ICs with 3 transistors or less with a single layer of interconnect [3,4]. Circuit complexity is limited with single-layer interconnects and metal-insulator-metal capacitors cannot be fabricated on-chip. Increasing the complexity of circuits while also increasing reliability at elevated temperature has been the focus of on-going work at NASA Glenn. This work reports the processing and testing of significantly more complex 4H-SiC JFET prototype ICs with two levels of metal interconnect capable of prolonged operation at 500 °C.

Fabrication

Fabrication was carried out on a commercially purchased 76 mm diameter 4H-SiC p-type wafer with epilayers [5] and employed interconnect technology with two layers of overlapping tantalum silicide ($TaSi_2$) insulated by silicon dioxide (SiO_2). As with prior work [3,4], the JFET gate and channel regions were defined by dry etching epilayers into isolation mesa patterns so that the dielectric and metal stack initiates from a non-planar SiC surface. Processing issues with non-planar topology have been found to compound as the number of non-planar steps increases. A field emission scanning electron micrograph (FESEM) image of the cross section of a fabricated JFET

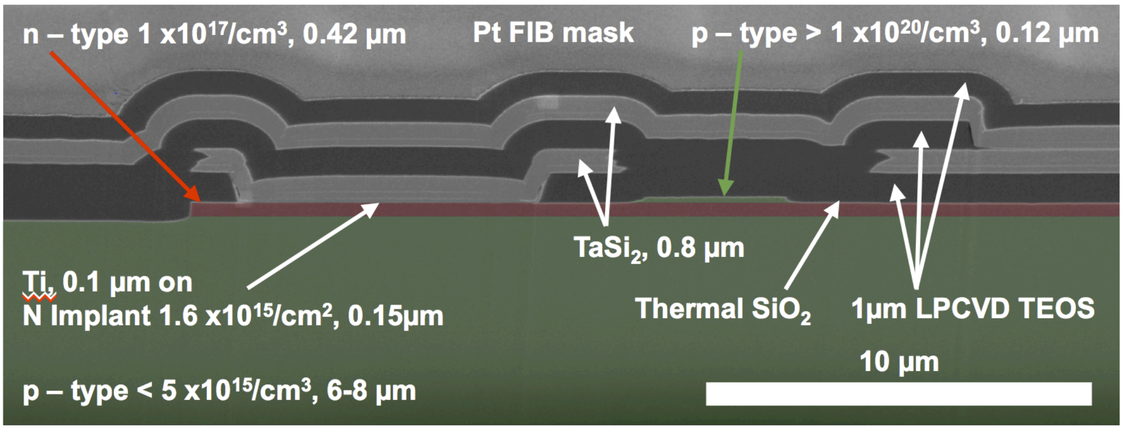

Fig. 1. FESEM image of a cross section prepared by FIB showing a 4H SiC JFET and two layer interconnect. The false color red and green shading was added to demark the various epi layers.

prepared by focus ion beam (FIB) can be seen in Fig. 1. The topmost gate mesa etch mask was also used for a self-aligned 70 keV nitrogen implant dose of 7.0 x 10^{12} cm^{-2} at room temperature. Silicon (Si) was e-beam deposited and patterned to form a mask for a nitrogen box-profile implant of 1.6 x 10^{15} cm^{-2} while heated to 600 °C to facilitate heavy doping for source/drain contacts. The wafer was capped with 1 µm of SiO_2 deposited at 720 °C by low-pressure chemical vapor deposition (LPCVD) using tetraethyl orthosilicate (TEOS) precursor before an activation anneal at 1360 °C in N_2 for 4 hours. The activation cap was stripped and two sequential short thermal oxidations of the wafer were grown and removed by 6:1 buffered oxide etchant (BOE). A third thermal oxide was grown 30 nm thick [6] and then coated with 1 µm TEOS LPCVD SiO_2 for the first dielectric layer. The contact via pattern was dry etched through most of the TEOS thickness with the remaining oxide removed by BOE. Device contacts to both n-implants and p^+ gates were made using 0.1 µm of sputtered Ti capped by $TaSi_2$, similar to the durable contact scheme first reported in [7]. TEOS LPCVD SiO_2 layers, 1 µm thick, were deposited between the $TaSi_2$ interconnects and between the topmost interconnect and bond pad metals. At elevated temperatures dielectric quality degrades and so thicker layers are needed [8]. $TaSi_2$ is employed as an interconnect metal to match the thermal coefficient of thermal expansion, improve adhesion, and achieve better chemical stability at elevated temperatures. A fairly thick trace is required to minimize the trace resistance and have enough metal to stop on in the next TEOS SiO_2 layer dry etch back. The $TaSi_2$ interconnects were deposited with a custom sputter system that allowed for a target to substrate spacing of 21 mm in order to minimize void formation over topologic features. Bond pads of tantalum silicide, platinum, iridium, and platinum ($TaSi_2$/Pt/Ir/Pt) were sequentially deposited and patterned via dry etching as described in [9]. The same $TaSi_2$/Pt/Ir/Pt metallization as

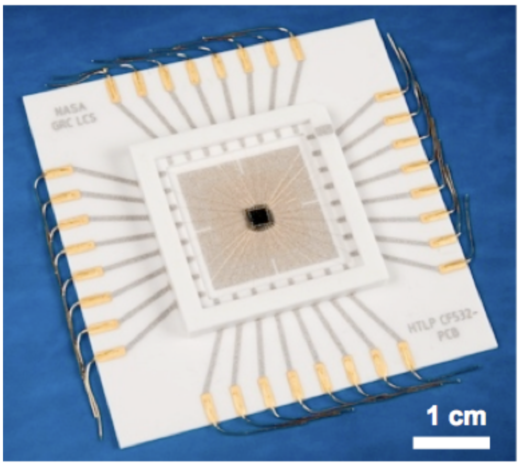

Fig. 2. Optical image of packaged Integrated Circuit.

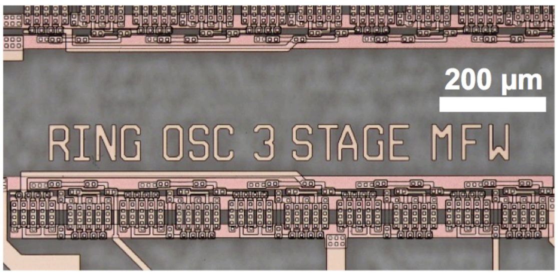

Fig. 3. Optical image of MF 3 stage ring oscillator. The two-levels of metal interconnect enables placement of power bus lines directly above underlying interconnects and transistors, which cuts the layout area of this circuit in half compared to single-level metal interconnect design.

the bond pads was used as a wafer backside contact. 1 µm of gold (Au) was deposited on the bond pads and back side and annealed for 10 hours in 4% forming gas.

The general circuit topology employed, which uses positive V_{DD} and negative V_{SS} power supplies and negative input/output voltages for both analog and digital signals, has been described elsewhere previously [4,10]. For digital circuits logic, high is usually a little below 0 V while logic low is more negative than -4 V, but actual values depend largely on epilayer threshold that grows increasingly negative as a function of radial distance from the wafer center [11]. Following probe-station electrical wafer-map testing, the wafer was saw-diced into 3mm x 3mm chips. A few selected chips were custom-packaged, some in 32-pin non hermetic high-temperature ceramic packages (Fig. 2), for prolonged electrical testing at 500 °C in room-air atmosphere oven [4,12].

Testing

Ring oscillators (such as the 10-transistor 3-stage oscillator shown in Fig. 3) were among the first ICs selected for 500 °C packaged testing, and are indicative of peak operating frequency for this process. Fig. 4 plots measured frequency as a function of 500° C testing time for four packaged oscillators of four different designs. Two of the four oscillators failed prior to 200 hours while one oscillator continued 500 °C functional testing through 3180 hours. Two individual NOT circuits of different designs operated 1160 hours and 2720 hours at 500 °C. An AND and NOR gate on the same chip with inputs tied to common pads lasted 220 hours and 240 hours, respectively. A separate set of NOT, NAND, and NOR circuits tied to common input pads collectively failed at 25 hours. These and other circuits tested to date yielded similar significant discrepancies in 500 °C operational durability. *Strong evidence of four distinct processing non-idealities believed responsible for the yield and 500 °C durability discrepancies observed in this work are reported in a separate submission to this conference proceedings [13].* Additionally, the room temperature wafer probe yield of a 0.5 mm^2 area 15 pF first metal/oxide/second metal on-chip capacitor was above 80%. The single on-chip capacitor that was packaged for high temperature durability testing survived 50% duty cycle 50 V/0V 20-hour stress cycles for 4300 hours at 500 °C before its measured 50 V 500 °C leakage current exceeded 1µA, as shown in Fig. 5.

Even more complex circuits than the ring oscillators worked at 500 °C, but with lower room-temperature yields and 500 °C durability. Fig. 6 shows 500 °C waveforms recorded during functional 500 °C testing of a packaged 16-transistor resistive ladder 4-bit digital to analog converter demonstration IC that operated for 10 hours. A prototype memory IC with a 24-transistor 4-bit address decoder driving a static RAM cell array operated for 120 hours at 500 °C (Fig. 7). A processing non-ideality described in [13] prevented successful reading of RAM array data at

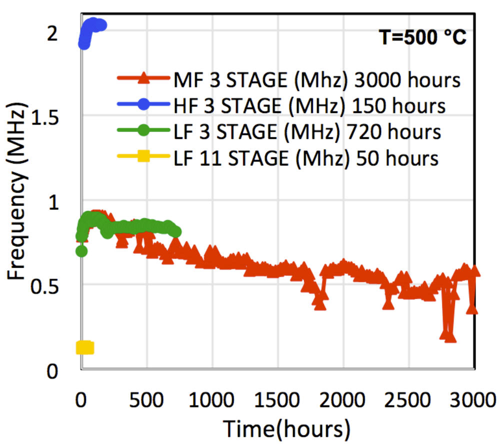

Fig. 4. Oscillation frequency vs. 500 °C operating time of four different ring oscillator designs.

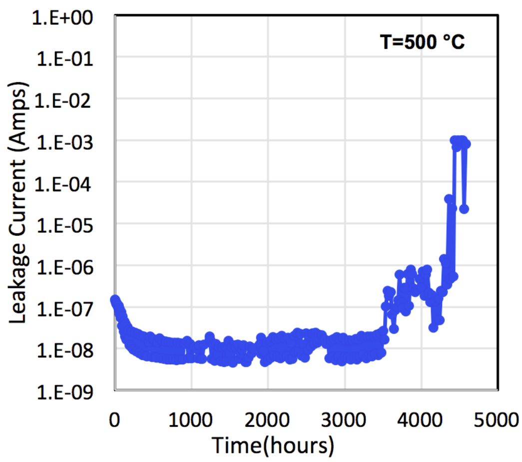

Fig. 5. Leakage current of a 15 pF capacitor with an area of 0.5 mm^2.

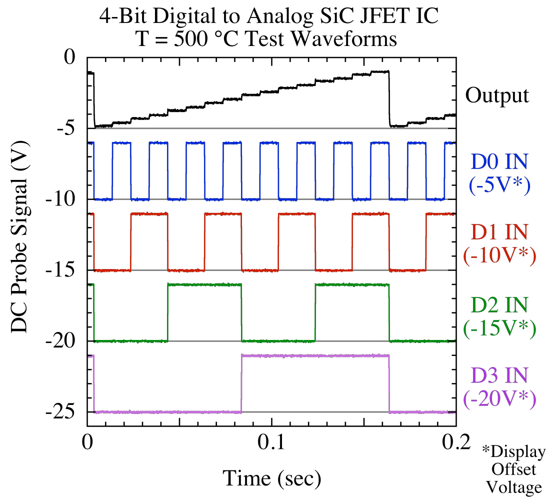

Fig. 6. D to A 500 °C test waveforms.

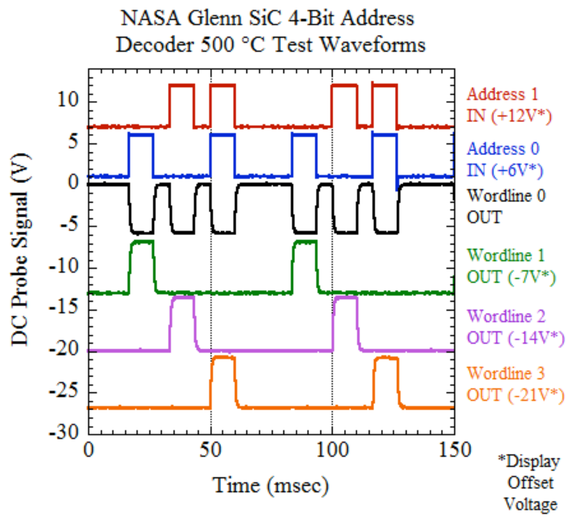

Fig. 7. 4-bit address decoder at 500 °C test waveforms.

500 °C. Nevertheless, the single RAM cell in the 4 bit x 4-bit test RAM array that was connected to a bonding pad for direct monitoring of its voltage demonstrated completely successful writing, storage, and reading of data at 500 °C.

Summary

This work demonstrates the possibility of 4H-SiC JFET circuits with multilayer interconnects achieving prolonged operation at 500 °C in air ambient. Further process improvements and design rule changes will be needed to make larger-scale multilayer interconnect integrated circuits routinely function at these extreme temperatures for even longer time periods [13]. Once larger-scale multilayer interconnect circuits have been fabricated with sufficient yield, more thorough reliability testing involving various temperatures, gas environments, and thermal cycling is planned.

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